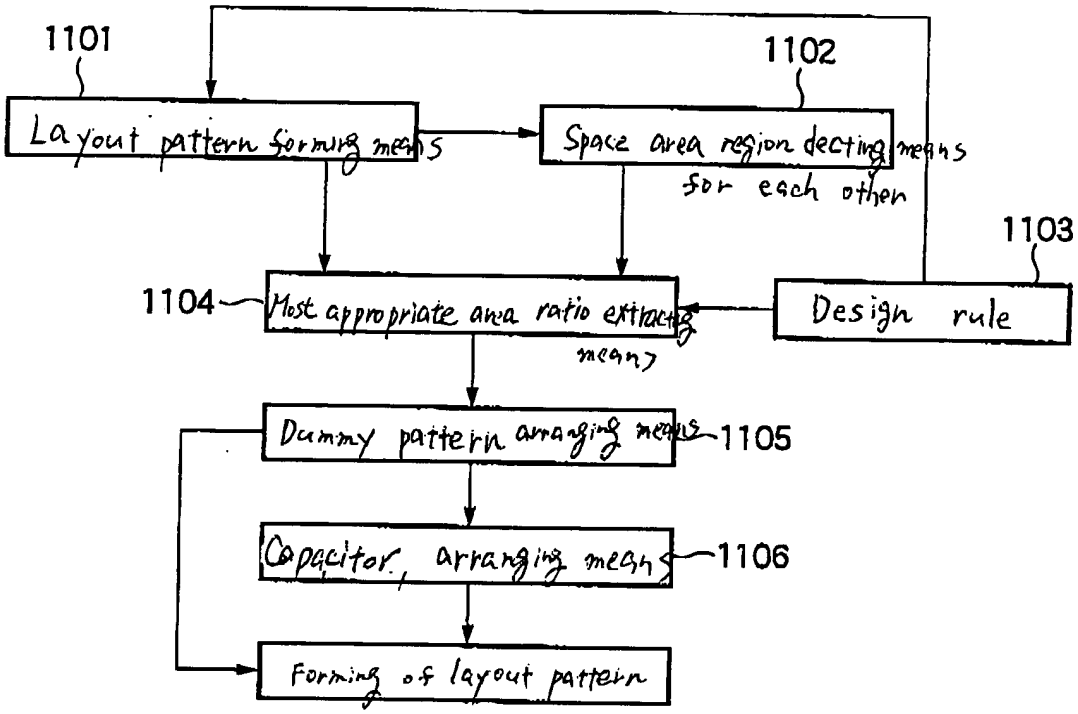
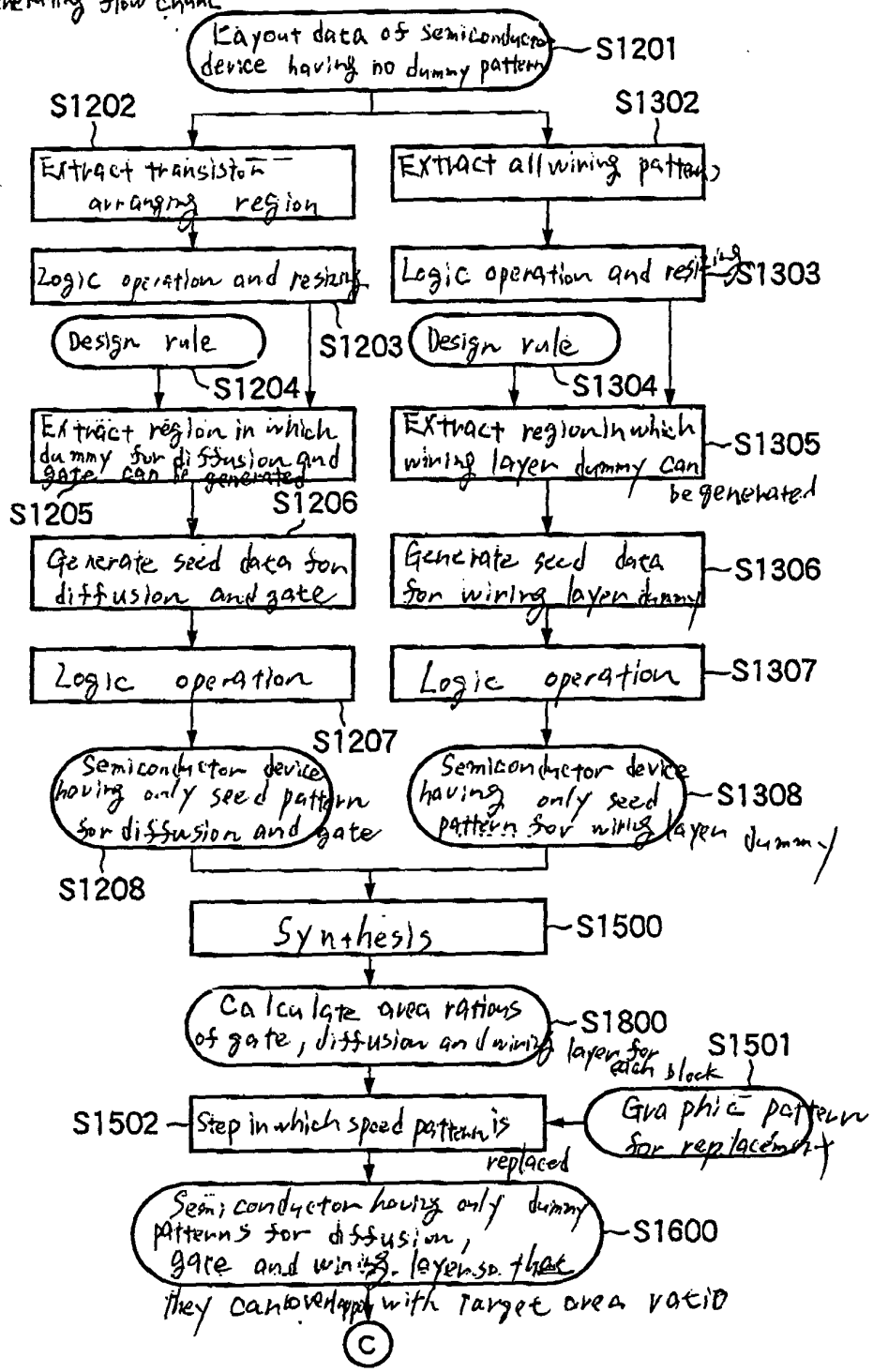
[Fig. 1]

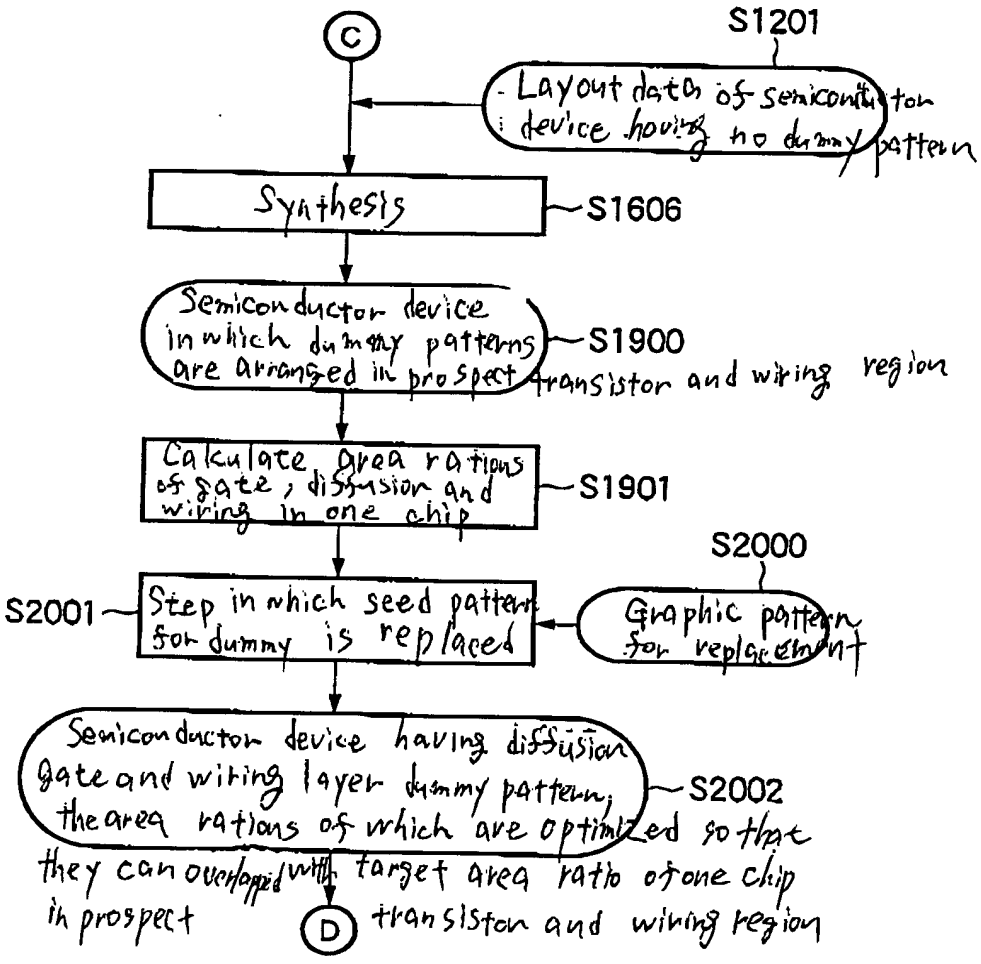

1101
1102
Layout pattern forming means
Space area region dectingmeans
for each other
1103
1104
Most appropriate area ratio extracting means
Design rule
Dummy pattern arranging means
1105
Capacitor arranging means
1106
Forming of layout pattern

[Fig.2]

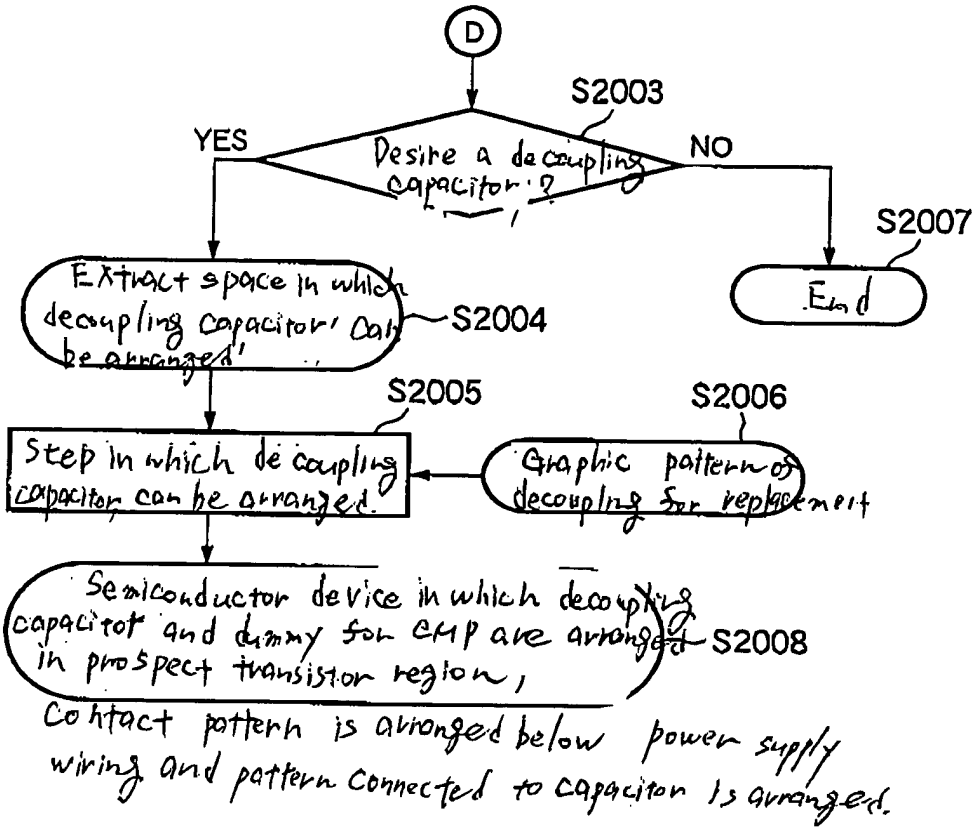
Dummy generating flow chart



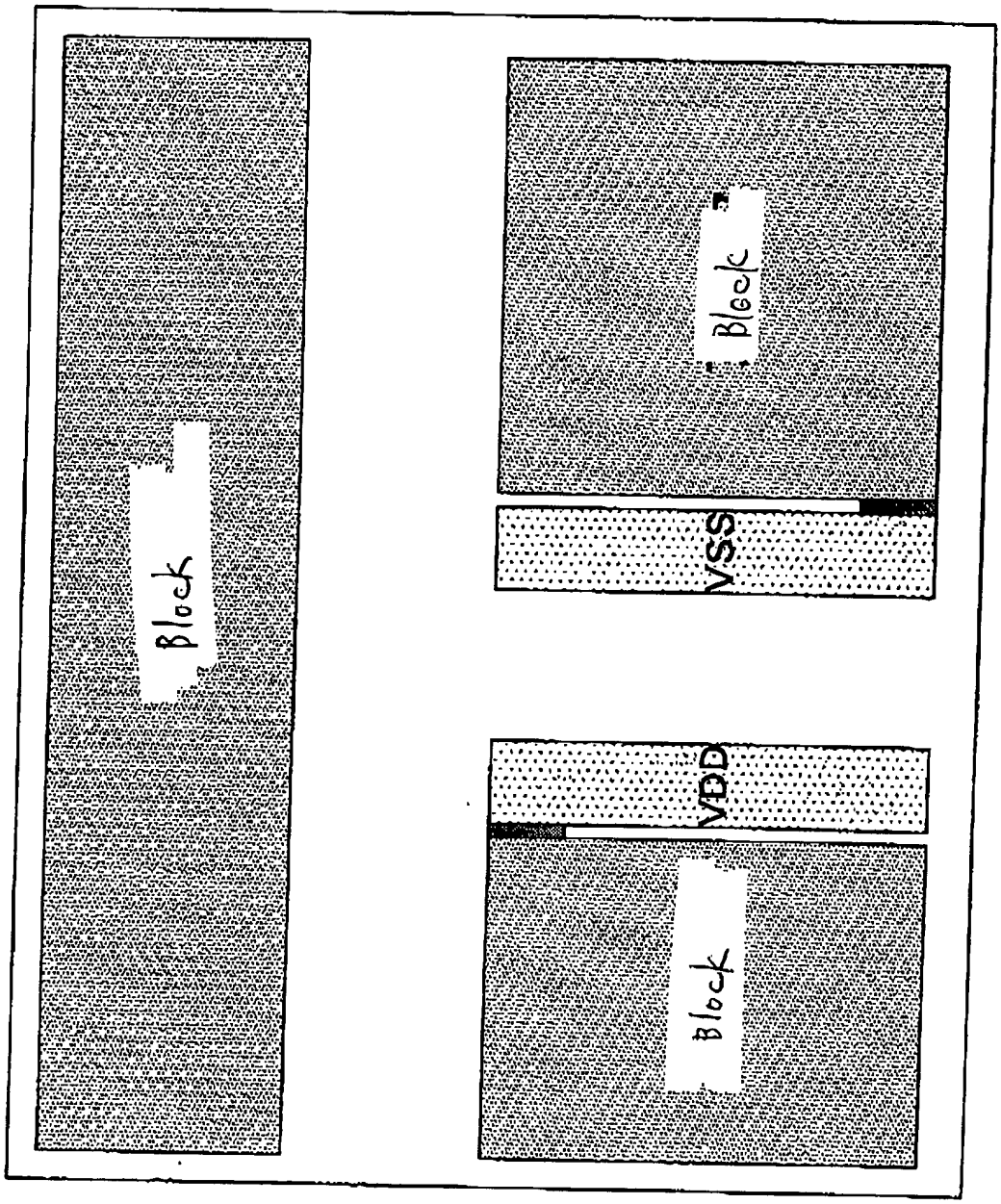
[Fig.3]


C
S1201
Layout data of semiconductor device having no dummy pattern
Synthesis
S1606
Semiconductor device in which dummy patterns are arranged in prospect
S1900
transistor and wiring region
Calculate area rations of gate, diffusion and wiring in one chip
S1901
S2000
S2001
Step in which seed pattern for dummy is replaced
Graphic pattern for replacement
Semiconductor device having diffusion gate and wiring layer dummy pattern, the area rations of which are optimized so that they can overlapped with target area ratio of one chip in prospect
S2002
D
transistor and wiring region

[Fig.4]


D
S2003
YES
Desire a decoupling capacitor?
NO
S2007
End
Extract space in which decoupling capacitor can be arranged
S2004
S2005
S2006
Step in which decoupling capacitor can be arranged.
Graphic pattern of decoupling for replacement
Semiconductor device in which decoupling capacitor and dummy for CMP are arranged in prospect transistor region,
S2008
Contact pattern is arranged below power supply wiring and pattern connected to capacitor is arranged.

[Fig. 5]



[Fig. 6]

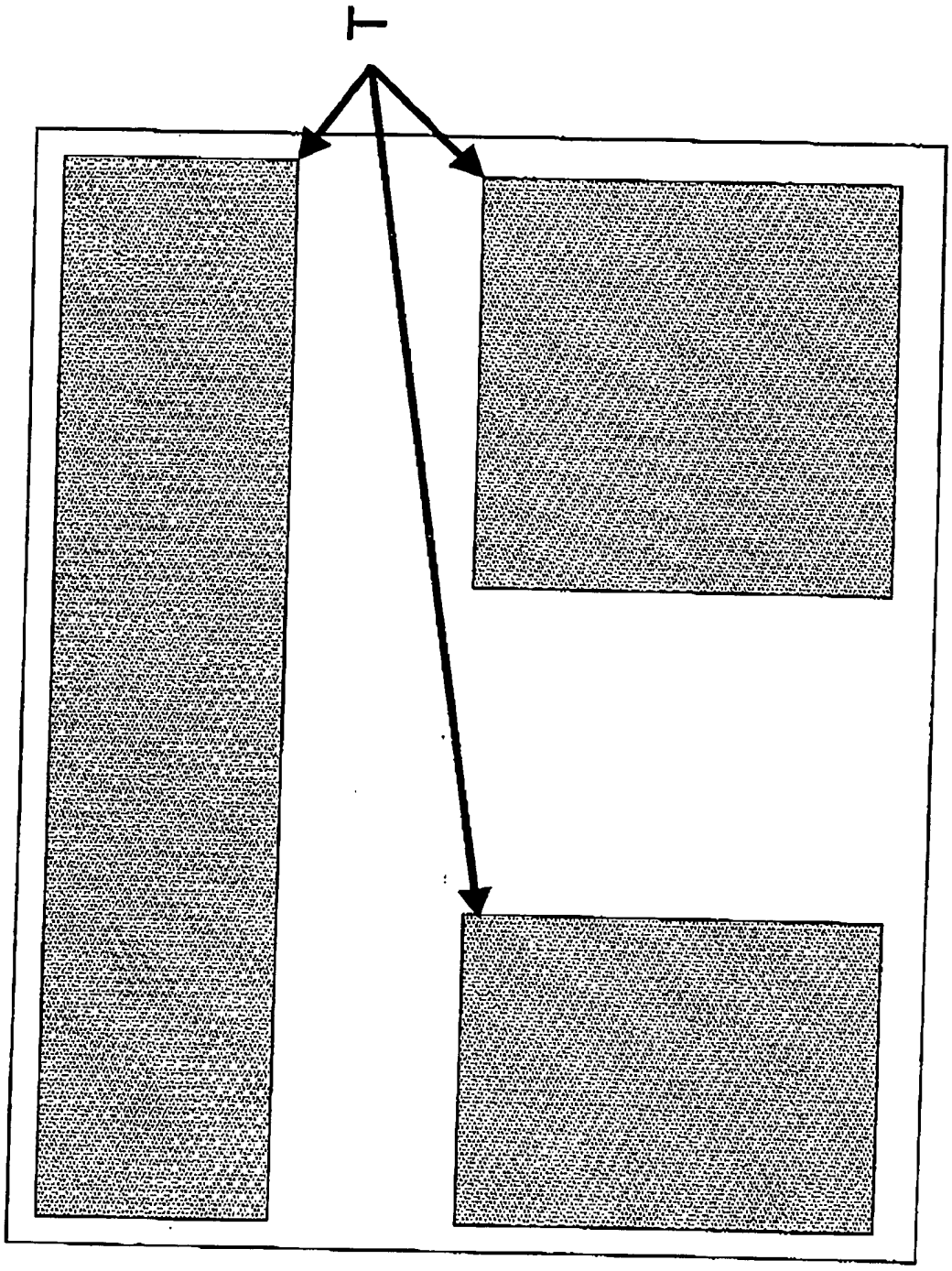


Fig. 7

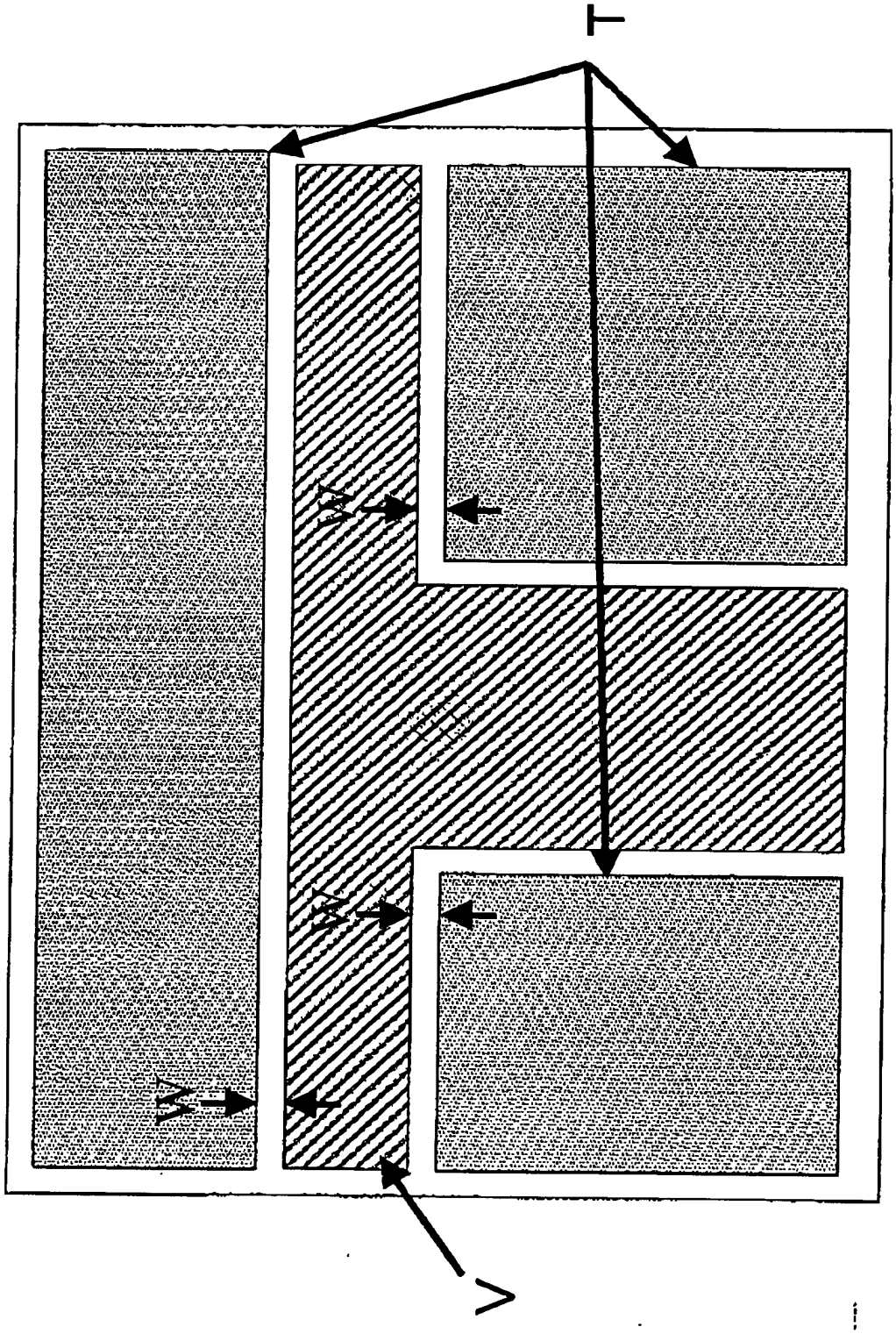
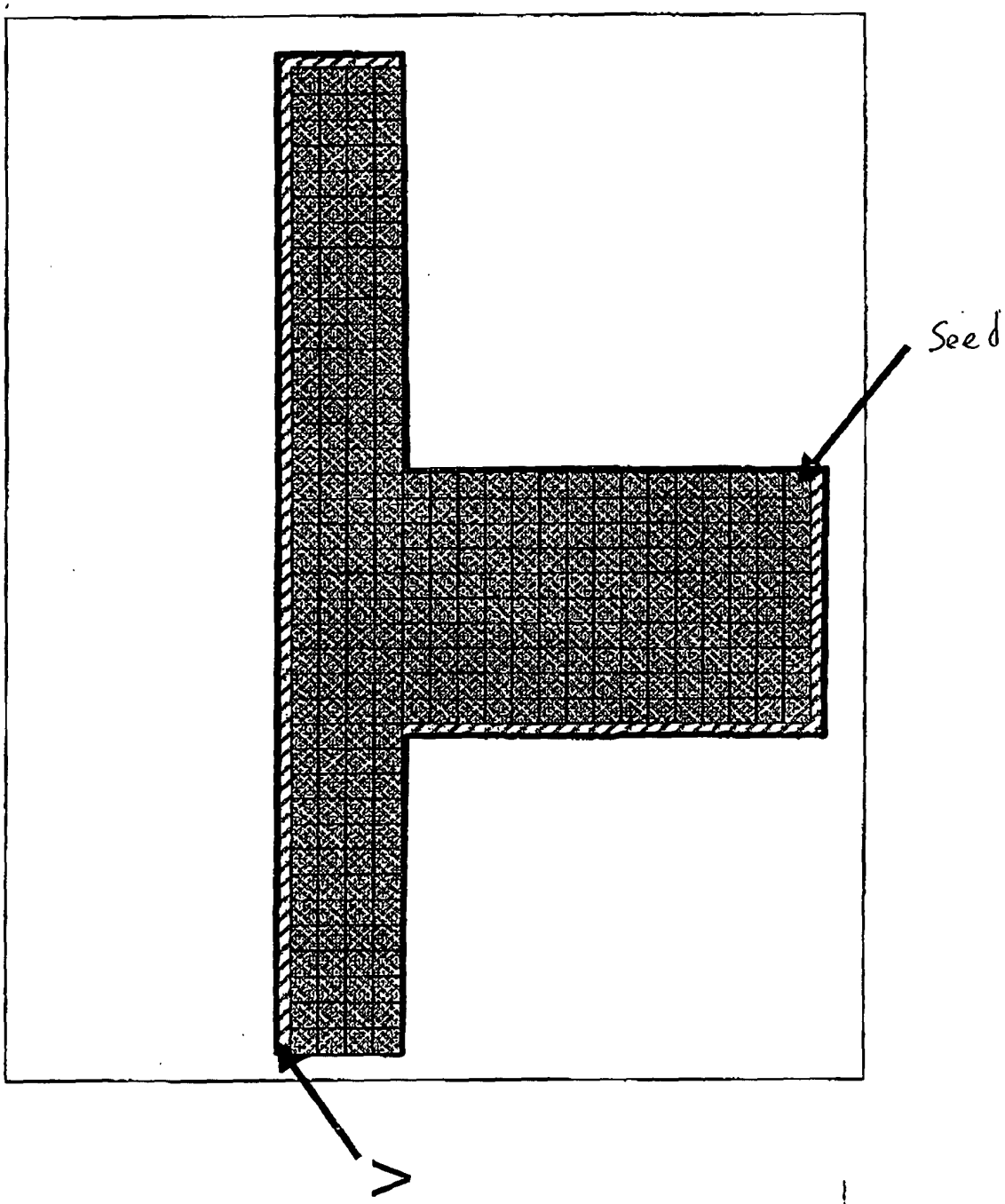


Fig. 8



[Fig. 9]

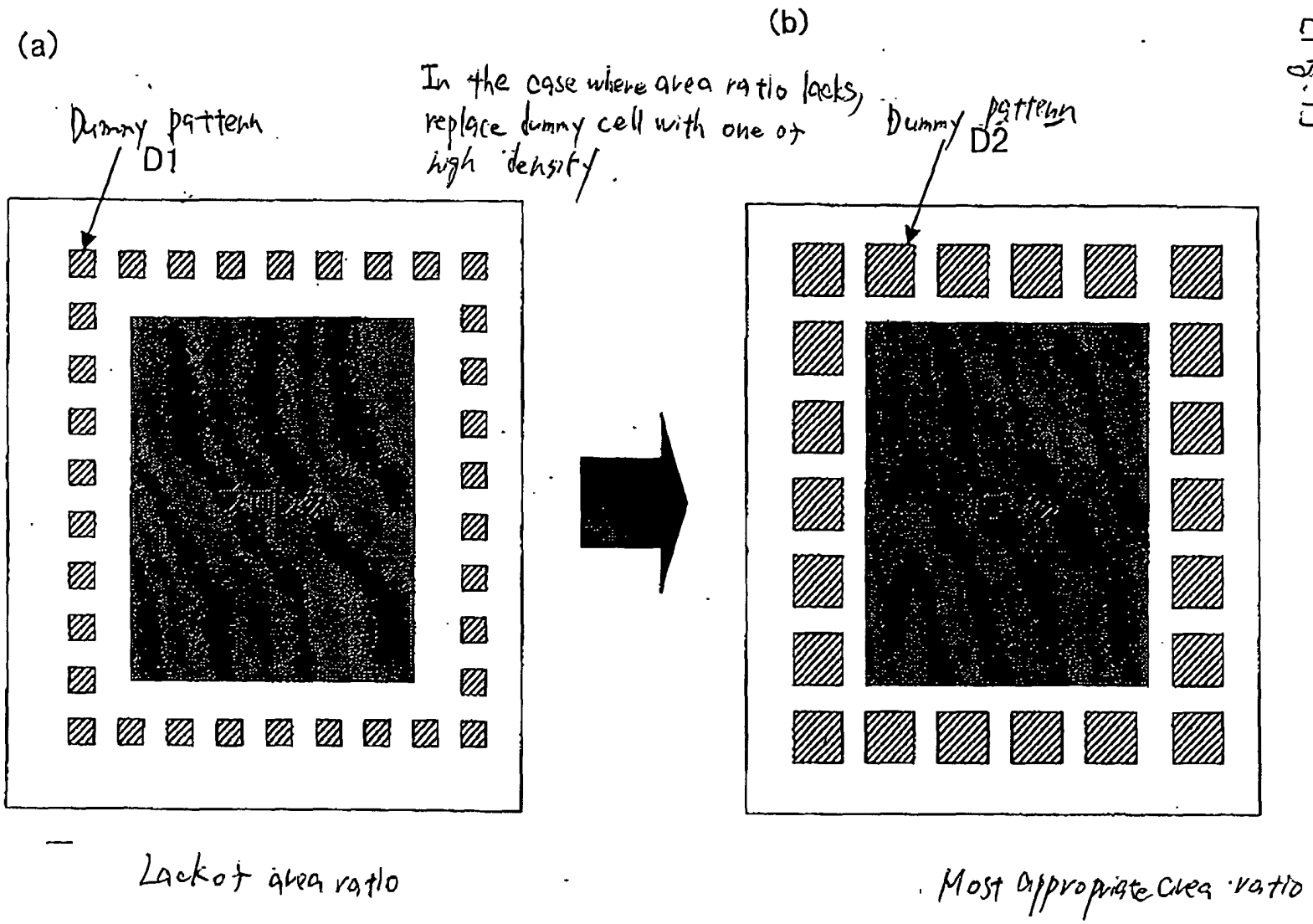


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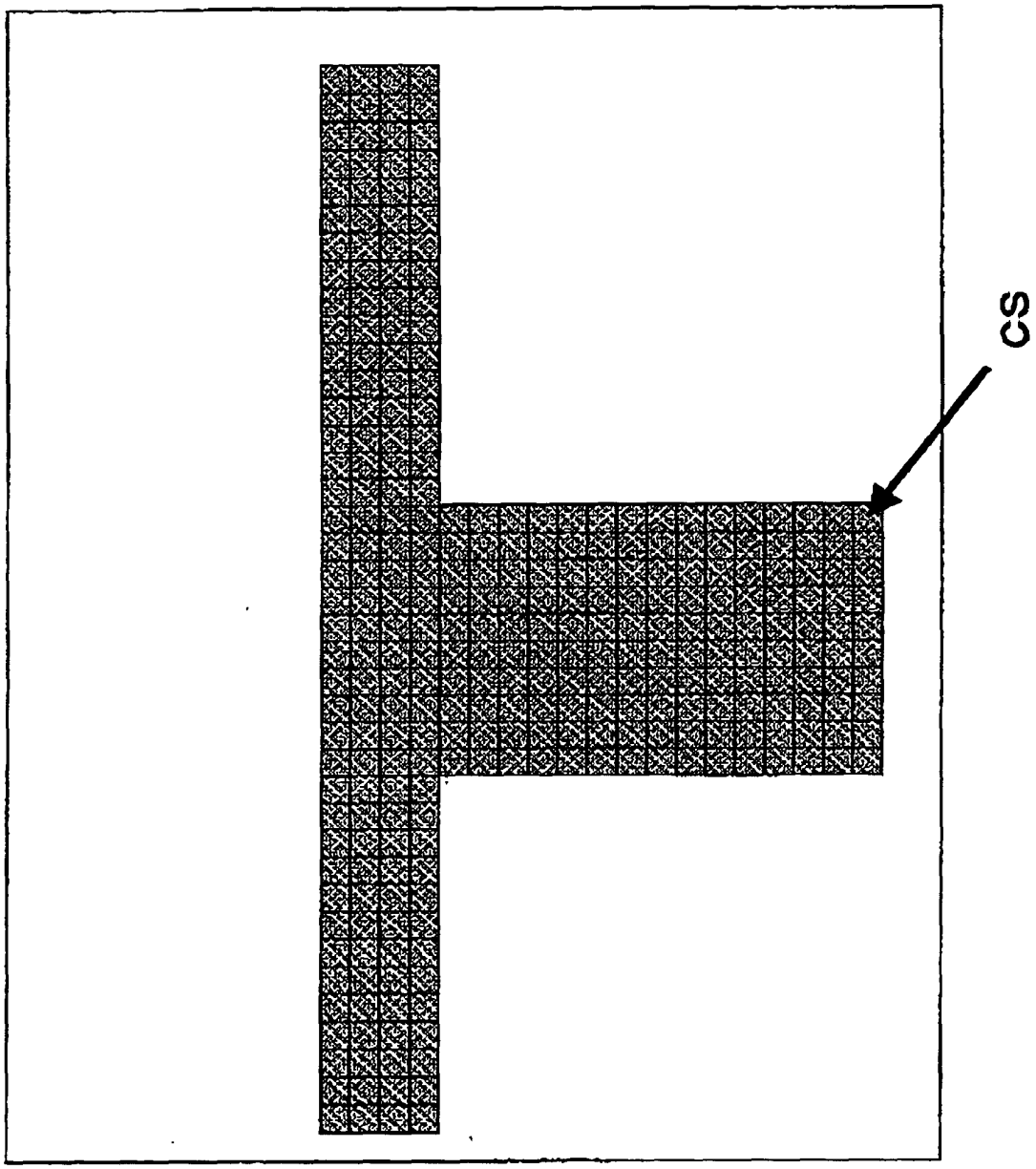
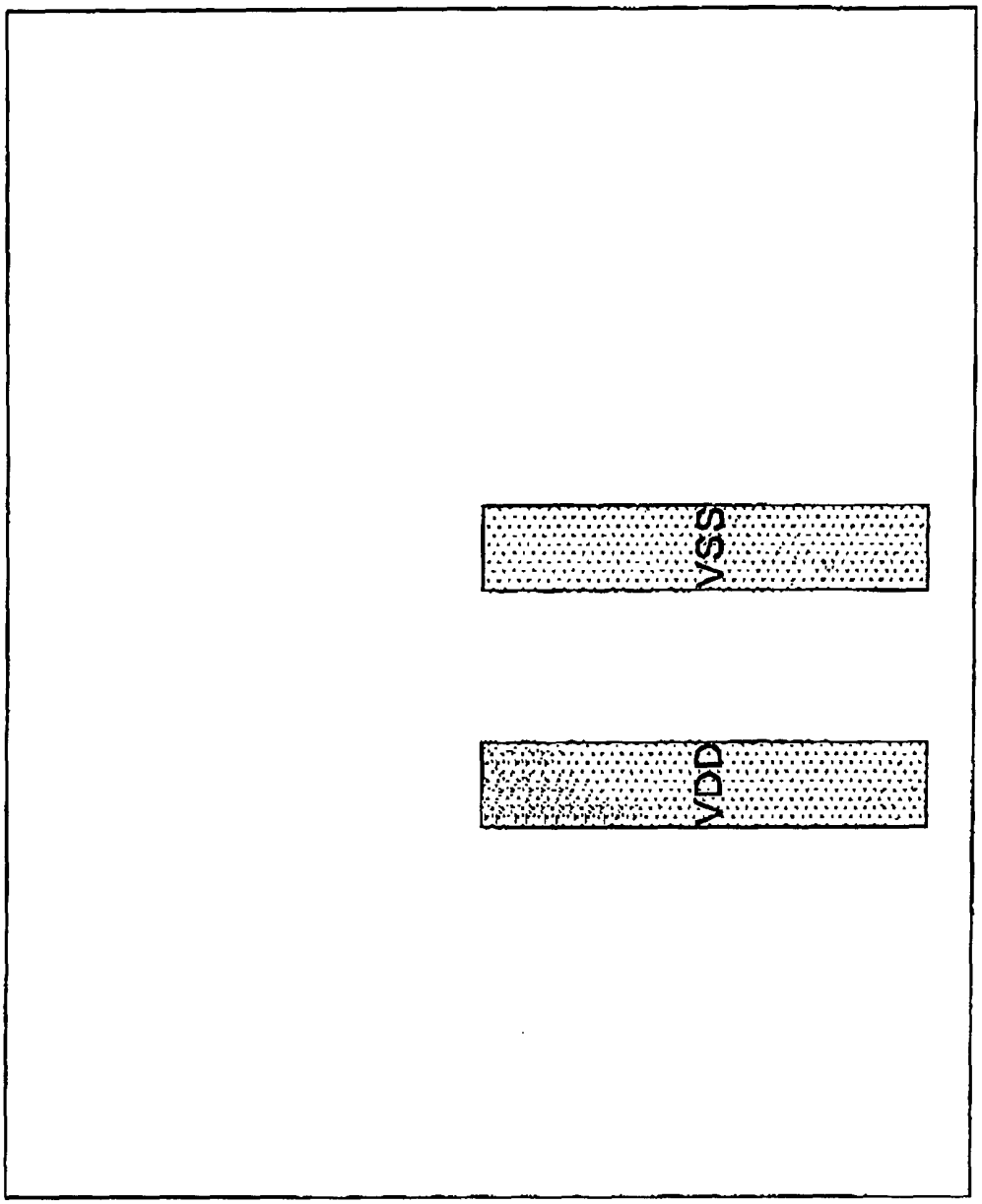
Fig.10



[Fig 11]



[Fig.13]

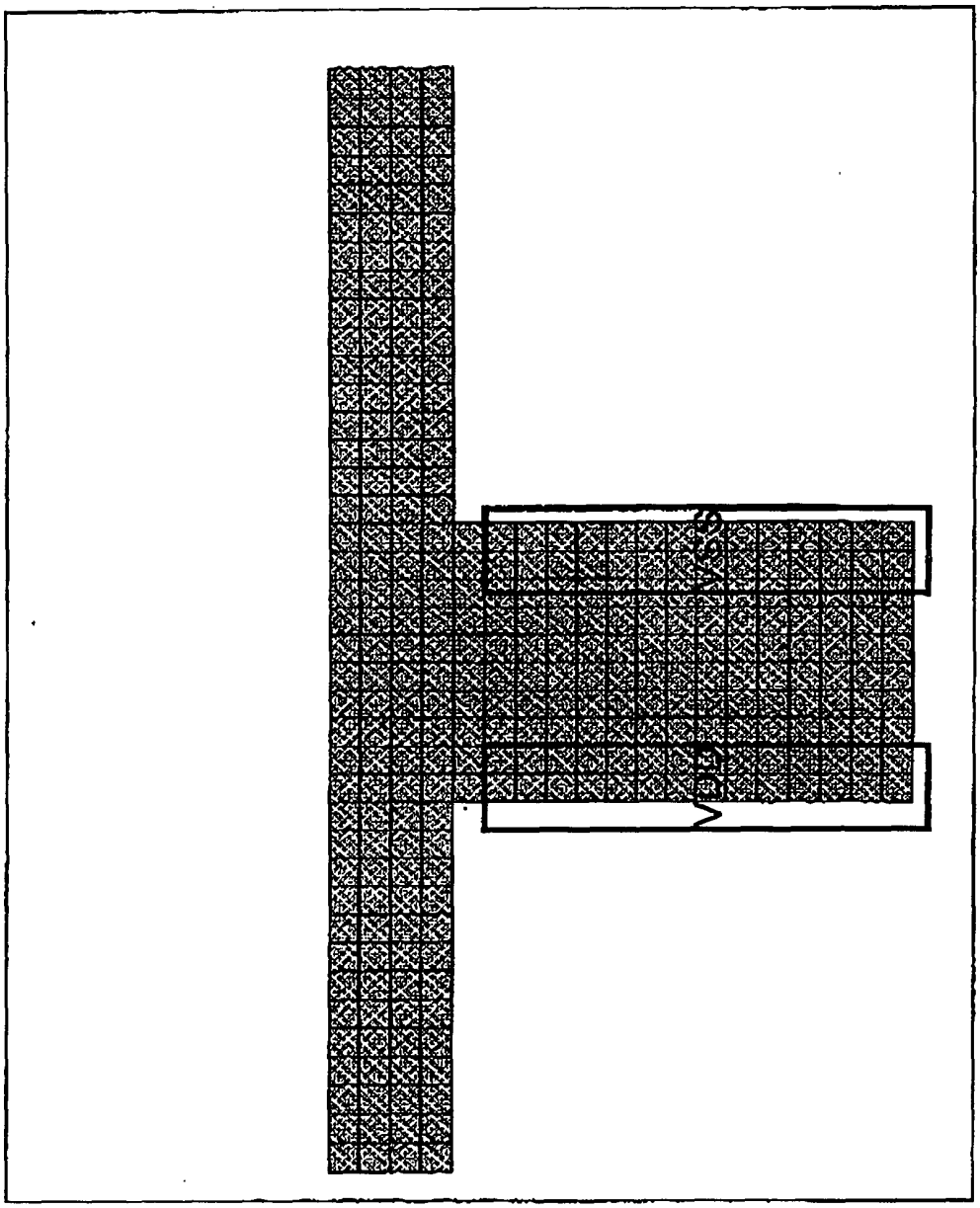
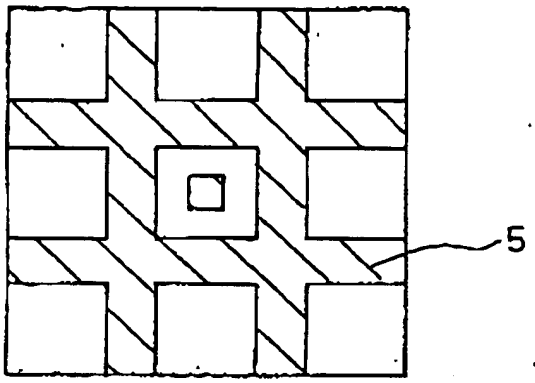
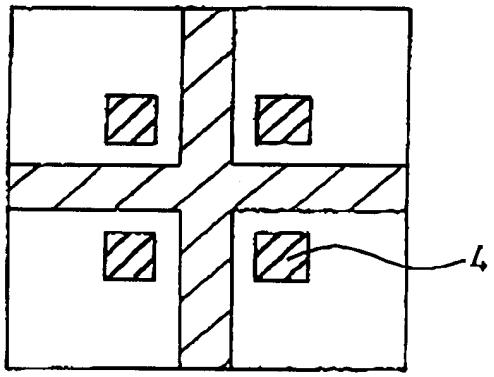


Fig. 13

(a)



(b)



(c)

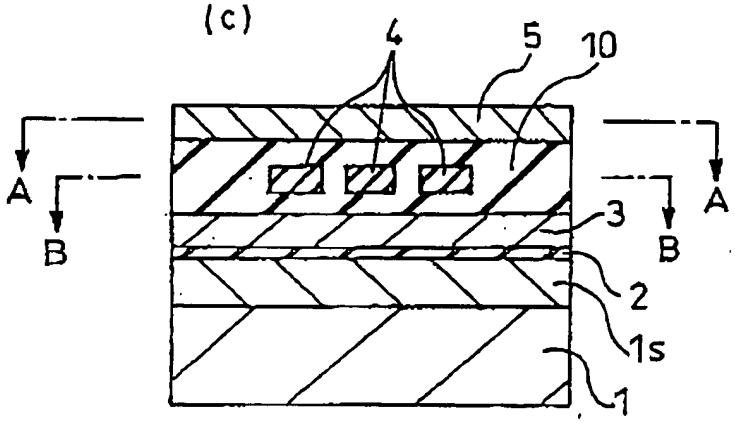
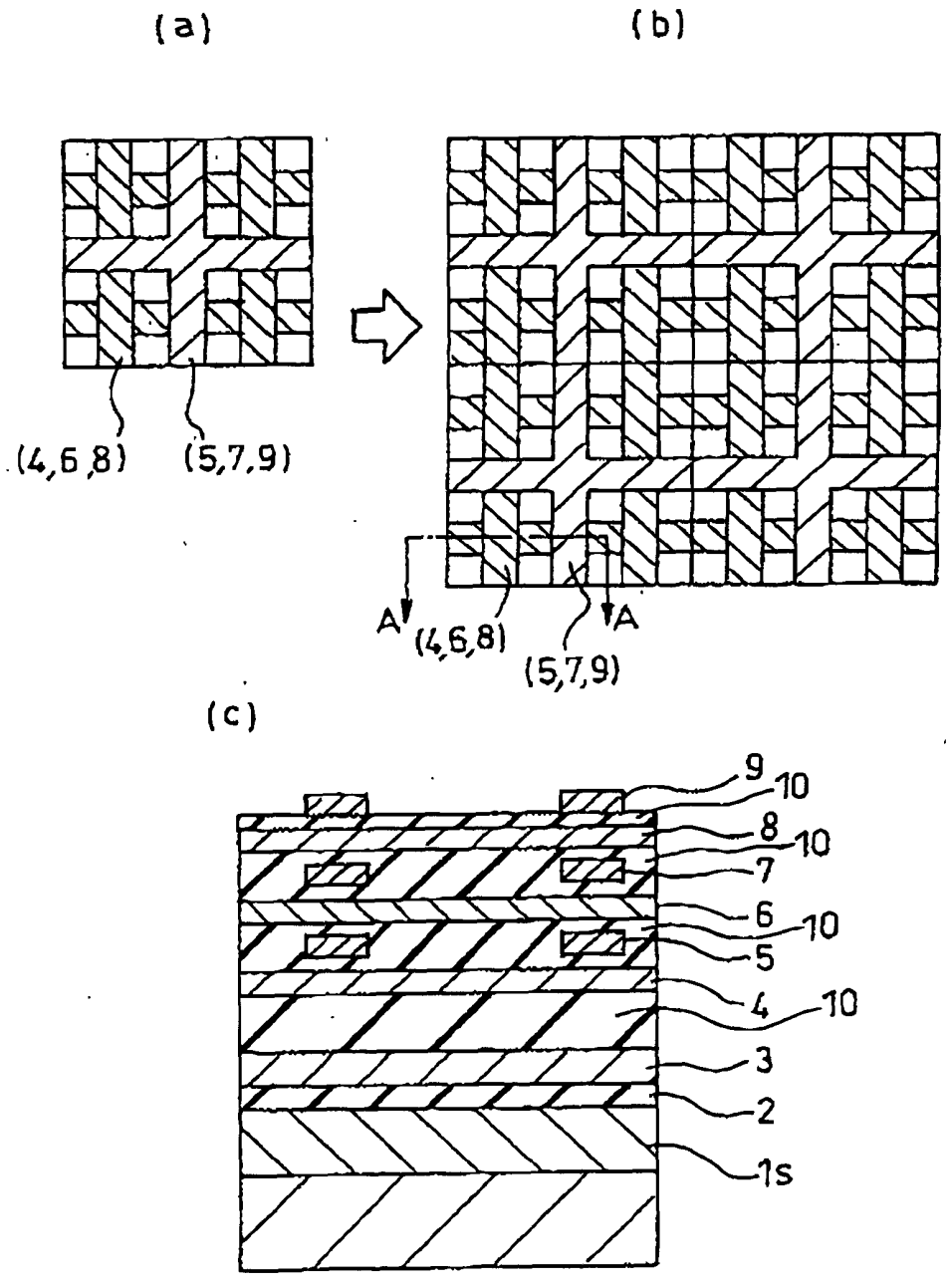
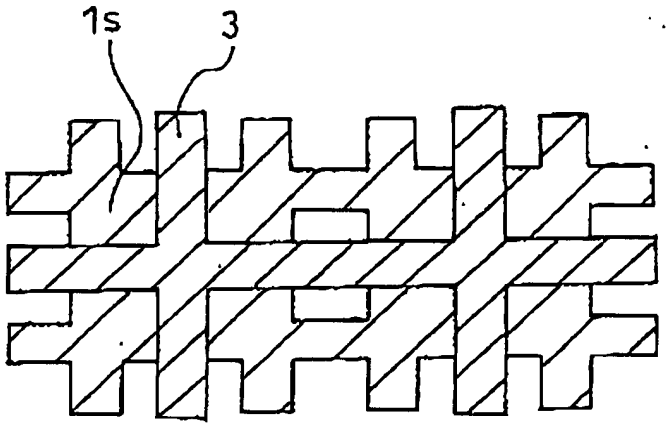


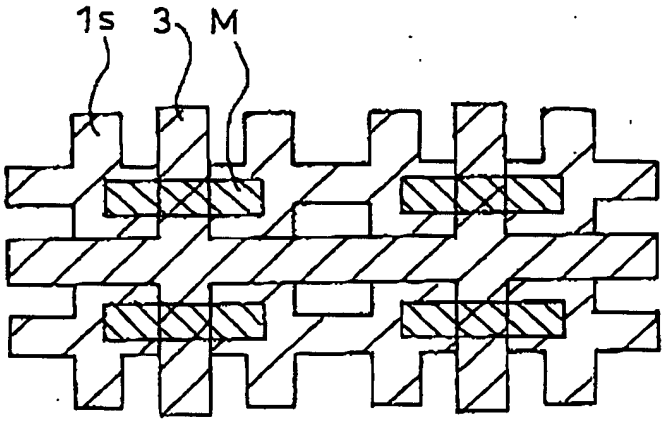
Fig.14



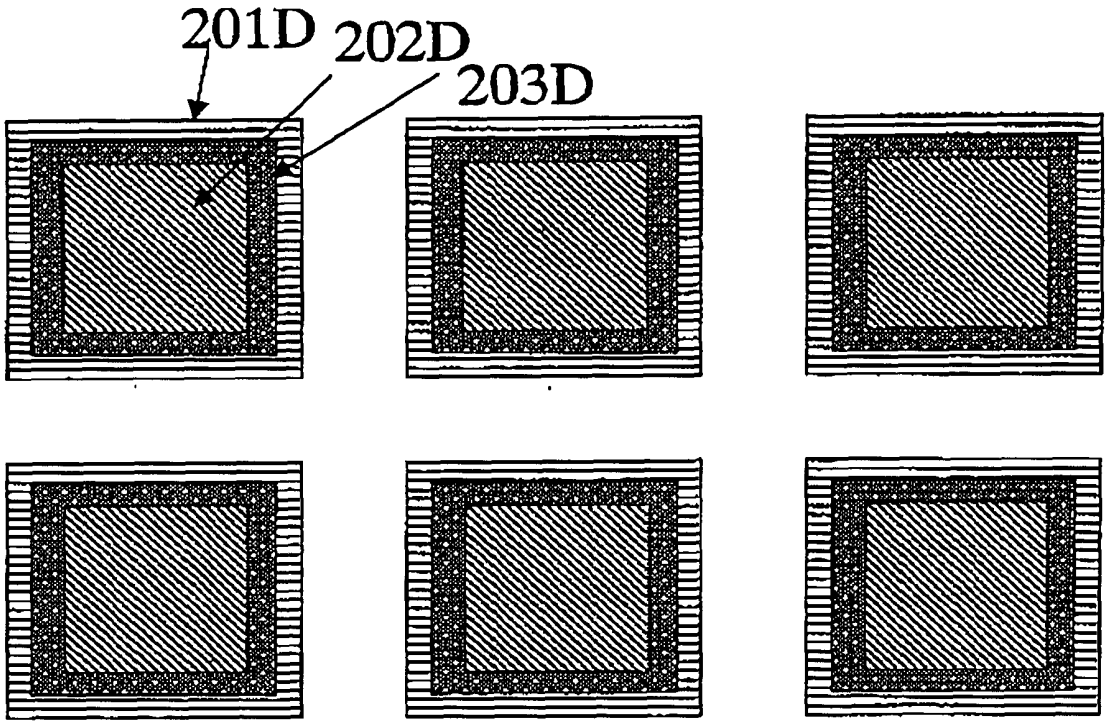
[Fig.15]



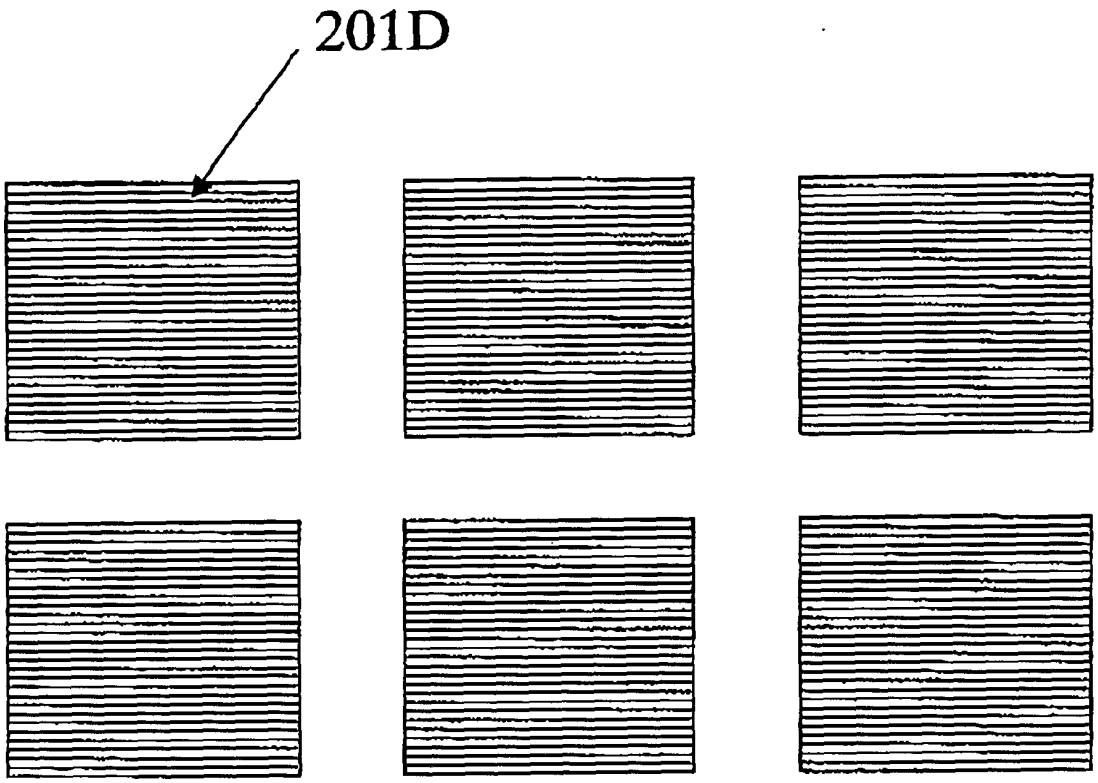
[Fig.16]



[Fig.17]



[Fig.18]



[Fig.19]

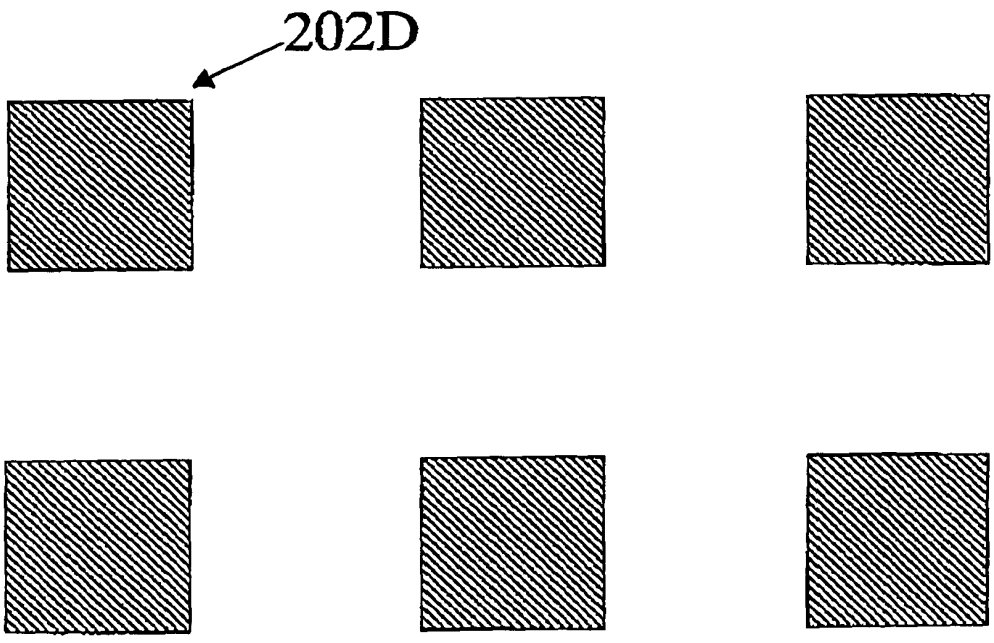
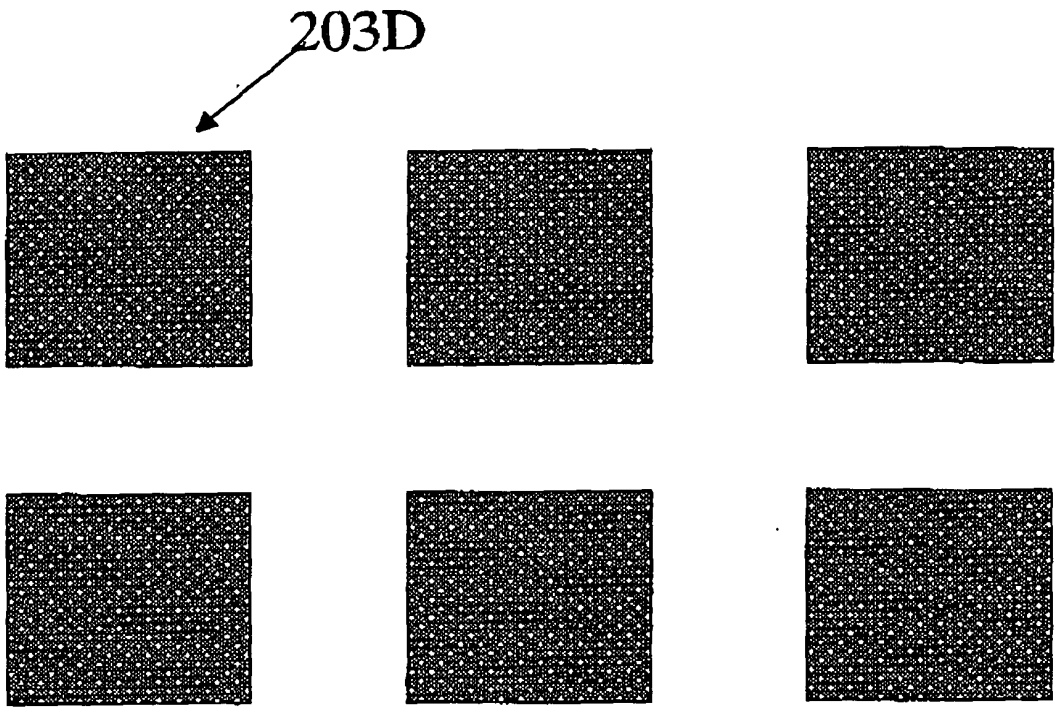


Fig.20



[Fig.2]

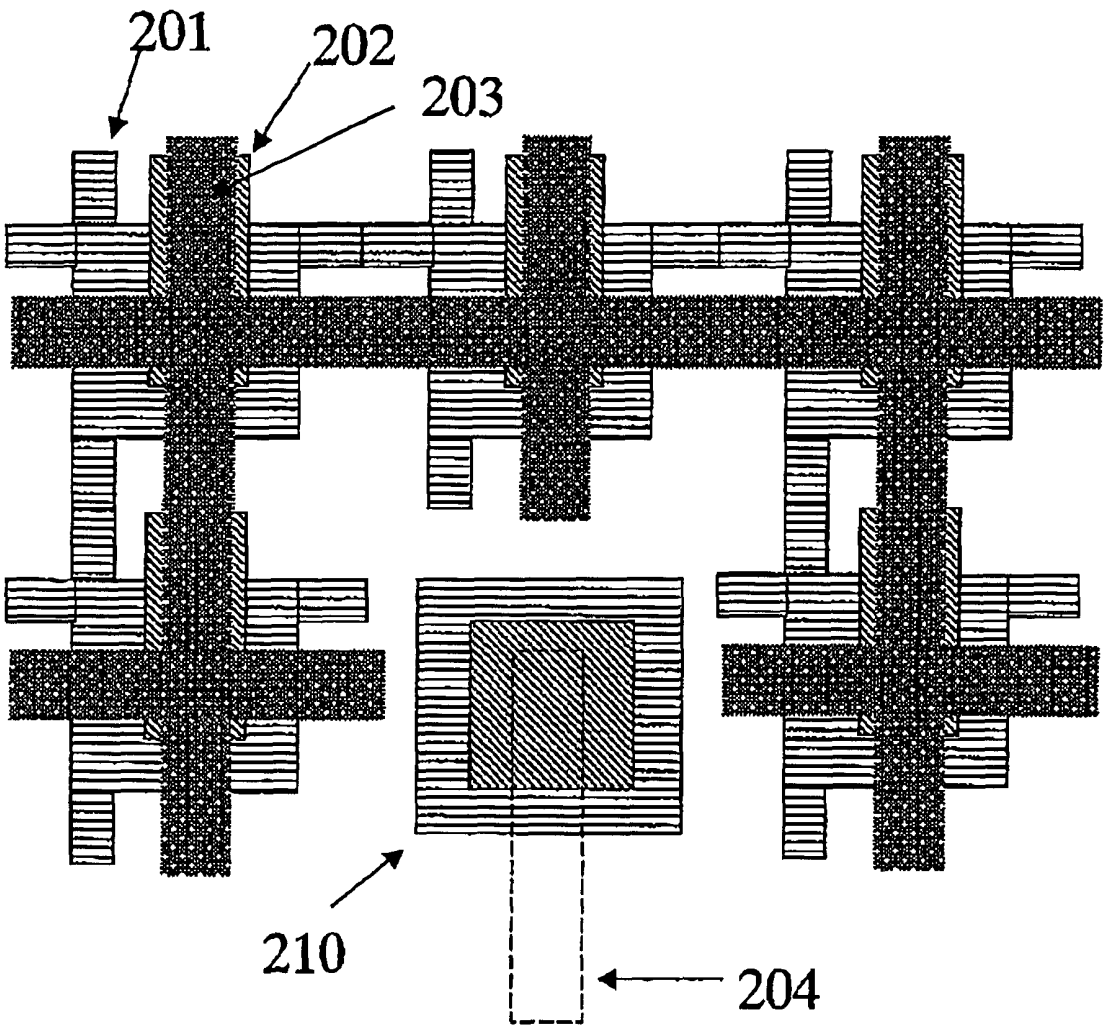


Fig.22

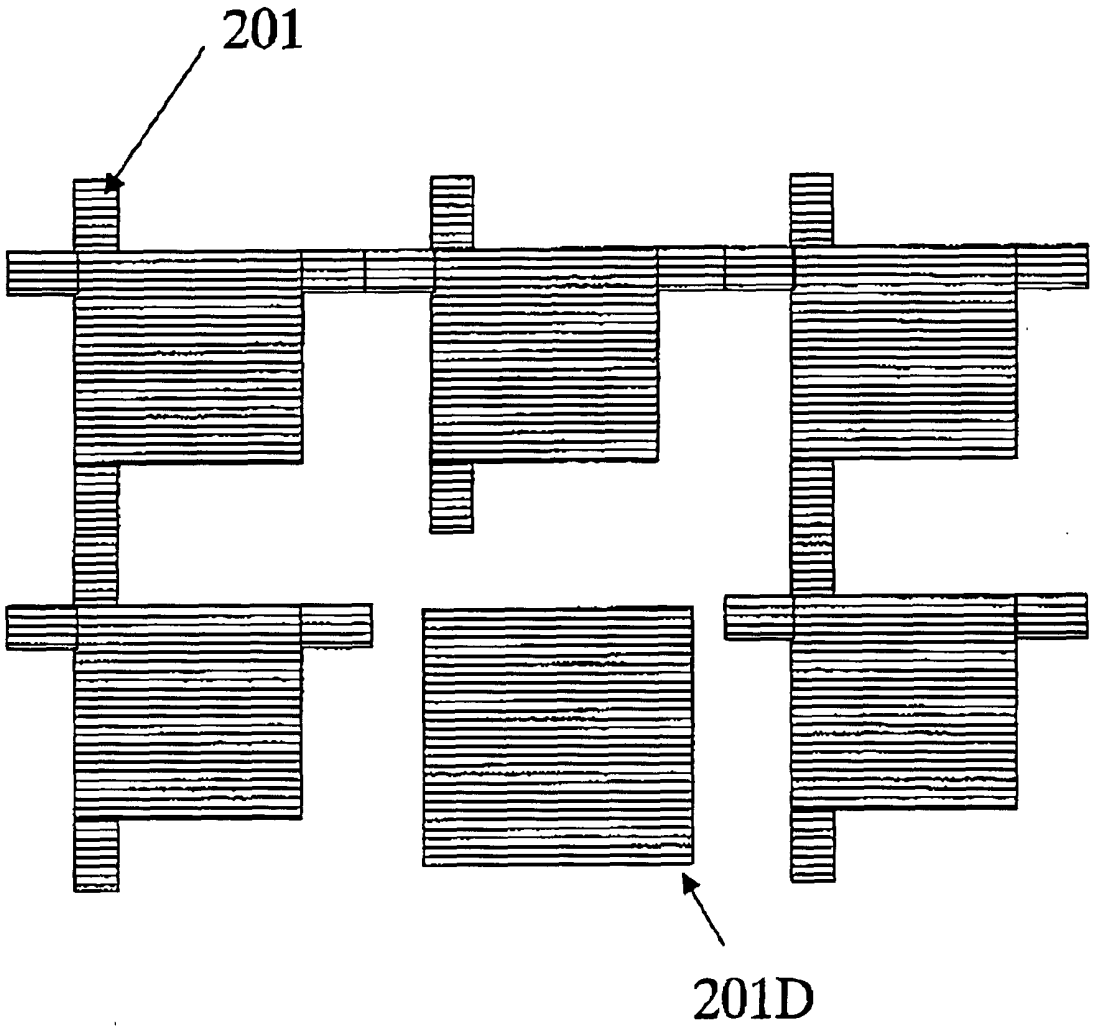
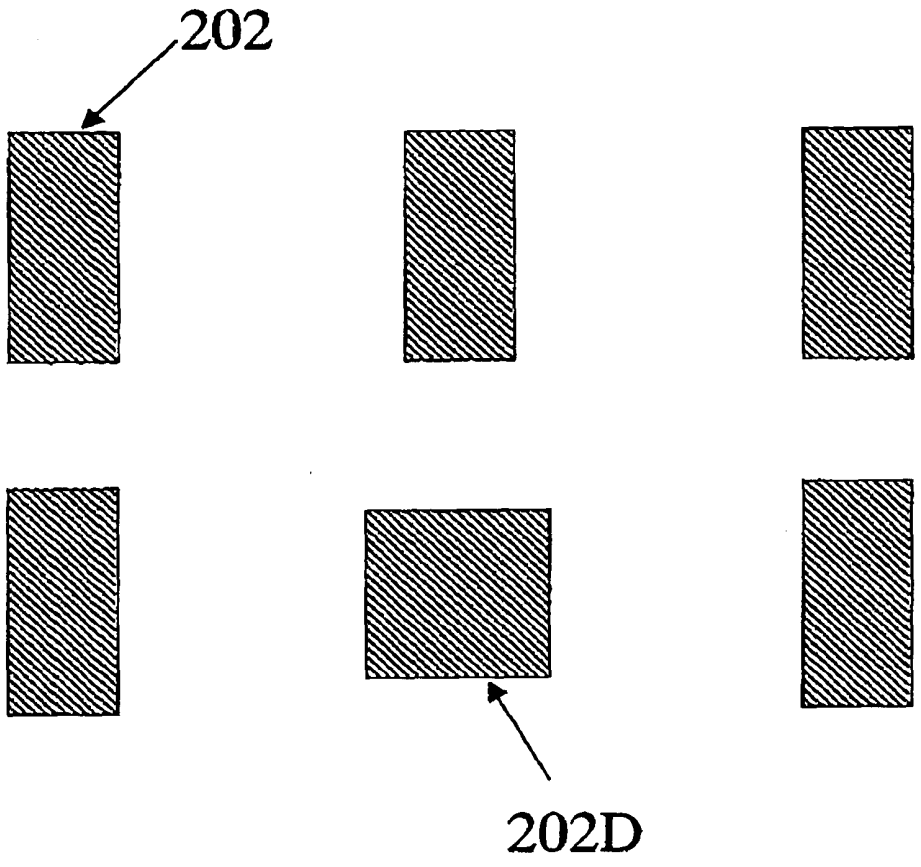
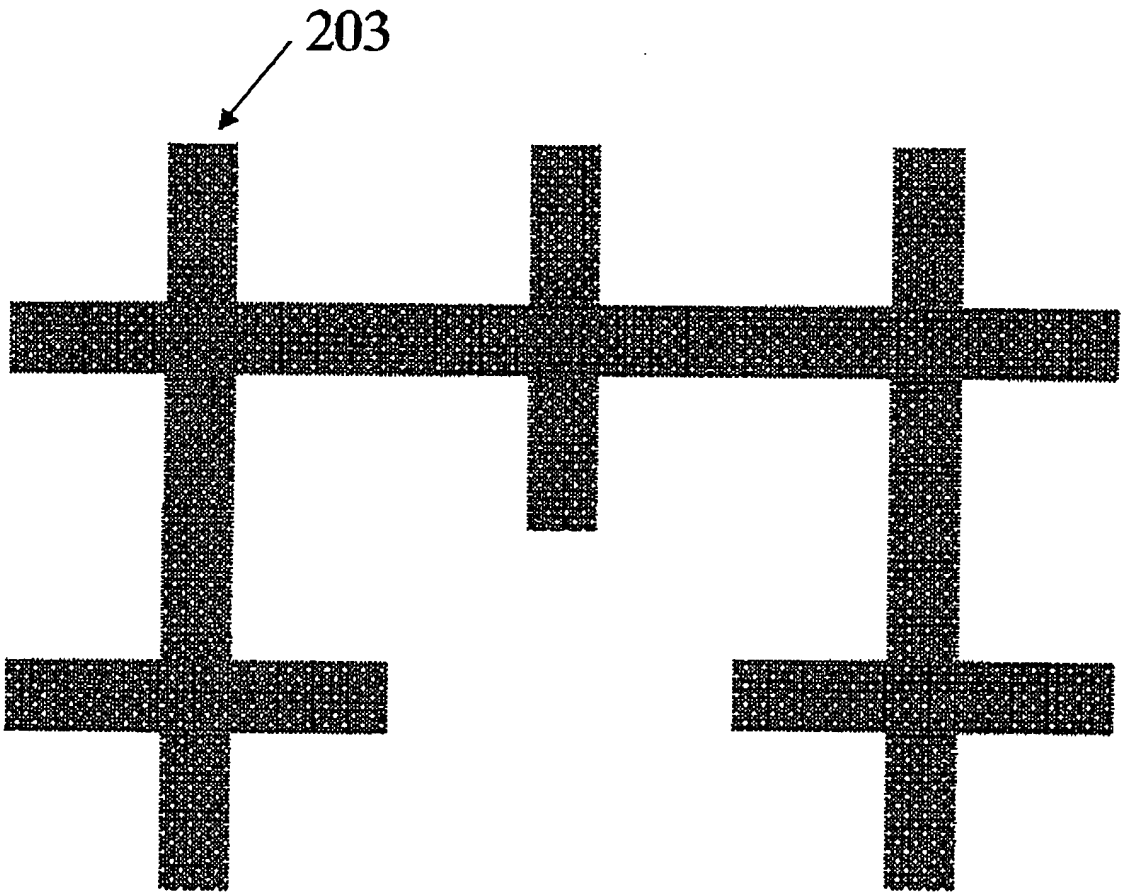


Fig.23



[Fig.29]